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02166766957 -02166766927

تهران پاساژ امجد طبقه1 واحد 16

info@atrinelec.com

@atrinelec

ANALOG DEVICES

Low Cost, Low Power Instrumentation Amplifier

AD620

FEATURES
EASY TO USE
Gain Set with One External Resistor
(Gain Range 1 to 1000)
Wide Power Supply Range (±2.3 V to ±18 V)
Higher Performance than Three Op Amp IA Designs
Available in 8-Lead DIP and SOIC Packaging
Low Power, 1.3 mA max Supply Current

EXCELLENT DC PERFORMANCE ("B GRADE")
50 μV max, Input Offset Voltage
0.6 μV/°C max, Input Offset Drift
1.0 nA max, Input Bias Current
100 dB min Common-Mode Rejection Ratio (G = 10)

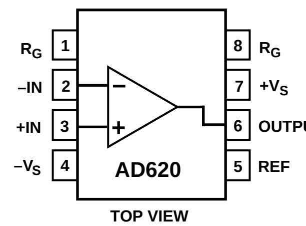
LOW NOISE
9 nV/√Hz, @ 1 kHz, Input Voltage Noise
0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
120 kHz Bandwidth (G = 100)
15 μs Settling Time to 0.01%

APPLICATIONS
Weigh Scales
ECG and Medical Instrumentation
Transducer Interface
Data Acquisition Systems
Industrial Process Controls
Battery Powered and Portable Equipment

CONNECTION DIAGRAM

8-Lead Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 1000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs, and offers lower power (only 1.3 mA max supply current), making it a good fit for battery powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max and offset drift of 0.6 μV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 μV p-p in the 0.1 Hz to 10 Hz band, 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01% and its cost is low enough to enable designs with one in-amp per channel.

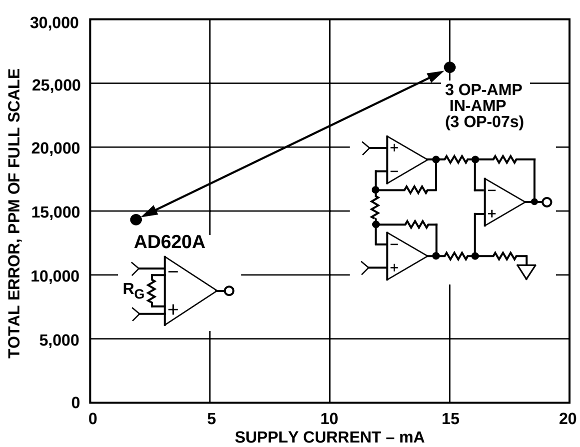


Figure 1. Three Op Amp IA Designs vs. AD620

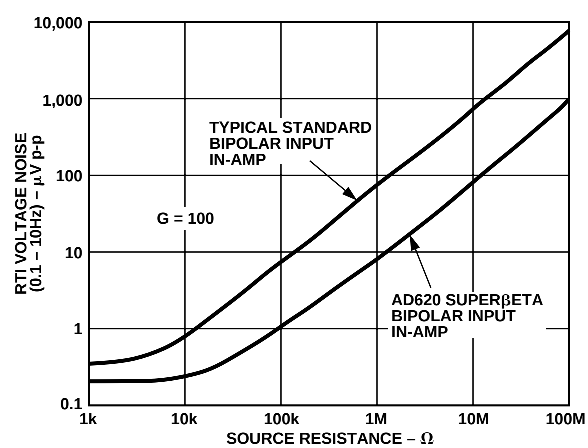


Figure 2. Total Voltage Noise vs. Source Resistance

REV. E

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

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AD620–SPECIFICATIONS (Typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
GAIN	G = 1 + (49.4 k/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error[2]	V_{OUT} = ±10 V										
G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity,	V_{OUT} = –10 V to +10 V,										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature											
	G =1			10			10			10	ppm/°C
	Gain >1[2]			–50			–50			–50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
Over Temperature	V_S = ±5 V to ±15 V			185			85			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ±5 V			1500			750			1500	µV
Over Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	µV
Average TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ‖pF
Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S + 1.9$		$+V_S - 1.2$	$-V_S + 1.9$		$+V_S - 1.2$	$-V_S + 1.9$		$+V_S - 1.2$	V
Over Temperature		$-V_S + 2.1$		$+V_S - 1.3$	$-V_S + 2.1$		$+V_S - 1.3$	$-V_S + 2.1$		$+V_S - 1.3$	V
	V_S = ±5 V to ±18 V	$-V_S + 1.9$		$+V_S - 1.4$	$-V_S + 1.9$		$+V_S - 1.4$	$-V_S + 1.9$		$+V_S - 1.4$	V
Over Temperature		$-V_S + 2.1$		$+V_S - 1.4$	$-V_S + 2.1$		$+V_S - 1.4$	$-V_S + 2.3$		$+V_S - 1.4$	V
Common-Mode Rejection Ratio DC to 60 Hz with I kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$-V_S + 1.1$		$+V_S - 1.2$	$-V_S + 1.1$		$+V_S - 1.2$	$-V_S + 1.1$		$+V_S - 1.2$	V
Over Temperature		$-V_S + 1.4$		$+V_S - 1.3$	$-V_S + 1.4$		$+V_S - 1.3$	$-V_S + 1.6$		$+V_S - 1.3$	V
	V_S = ±5 V to ±18 V	$-V_S + 1.2$		$+V_S - 1.4$	$-V_S + 1.2$		$+V_S - 1.4$	$-V_S + 1.2$		$+V_S - 1.4$	V
Over Temperature		$-V_S + 1.6$		$+V_S - 1.5$	$-V_S + 1.6$		$+V_S - 1.5$	$-V_S + 2.3$		$+V_S - 1.5$	V
Short Current Circuit			±18			±18			±18		mA

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
DYNAMIC RESPONSE											
Small Signal –3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		µs
G = 1000			150			150			150		µs
NOISE											
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e^2{}_{ni}) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	µV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	µV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range[4]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			–40 to +85			–40 to +85			–55 to +125		°C

NOTES
[1]See Analog Devices military data sheet for 883B tested specifications.
[2]Does not include effects of external resistor R_G.
[3]One input grounded. G = 1.
[4]This is defined as the same supply range which is used to specify PSR.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2] . . . . 650 mW
Input Voltage (Common Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . ±25 V
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range (Q) . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range
  AD620 (A, B) . . . . −40°C to +85°C
  AD620 (S) . . . . −55°C to +125°C
Lead Temperature Range
  (Soldering 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Lead Plastic Package: θ_{JA} = 95°C/W
8-Lead Cerdip Package: θ_{JA} = 110°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W

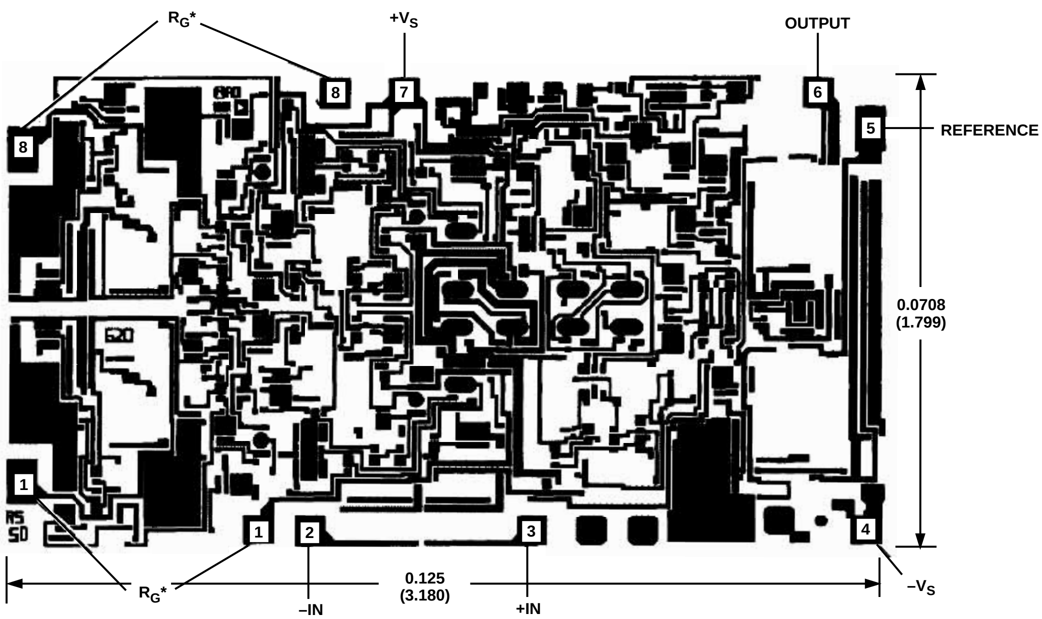
ORDERING GUIDE

Model	Temperature Ranges	Package Options*
AD620AN	−40°C to +85°C	N-8
AD620BN	−40°C to +85°C	N-8
AD620AR	−40°C to +85°C	SO-8
AD620AR-REEL	−40°C to +85°C	13" REEL
AD620AR-REEL7	−40°C to +85°C	7" REEL
AD620BR	−40°C to +85°C	SO-8
AD620BR-REEL	−40°C to +85°C	13" REEL
AD620BR-REEL7	−40°C to +85°C	7" REEL
AD620ACHIPS	−40°C to +85°C	Die Form
AD620SQ/883B	–55°C to +125°C	Q-8

*N = Plastic DIP; Q = Cerdip; SO = Small Outline.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



*FOR CHIP APPLICATIONS: THE PADS $1R_G$ AND $8R_G$ MUST BE CONNECTED IN PARALLEL TO THE EXTERNAL GAIN REGISTER R_G. DO NOT CONNECT THEM IN SERIES TO R_G. FOR UNITY GAIN APPLICATIONS WHERE R_G IS NOT REQUIRED, THE PADS $1R_G$ MAY SIMPLY BE BONDED TOGETHER, AS WELL AS THE PADS $8R_G$.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD620 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Characteristics (@ +25°C, $V_S = \pm 15$ V, $R_L = 2$ kΩ, unless otherwise noted)

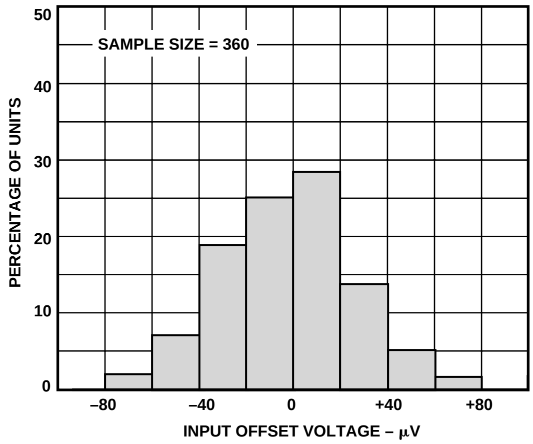


Figure 3. Typical Distribution of Input Offset Voltage

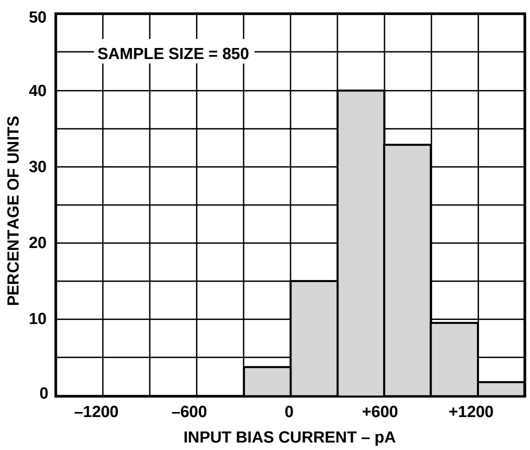


Figure 4. Typical Distribution of Input Bias Current

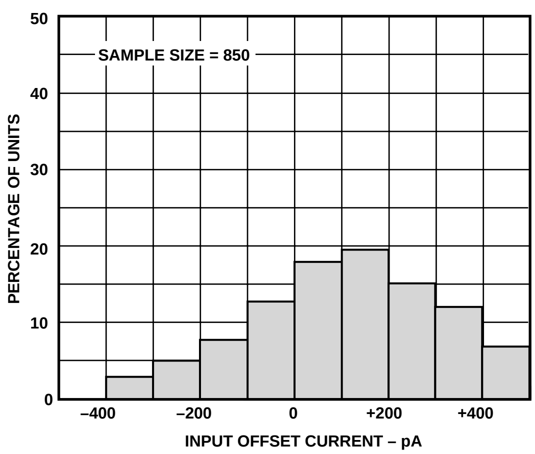


Figure 5. Typical Distribution of Input Offset Current

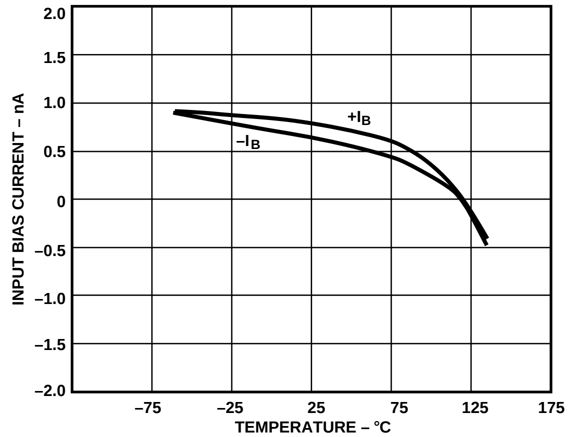


Figure 6. Input Bias Current vs. Temperature

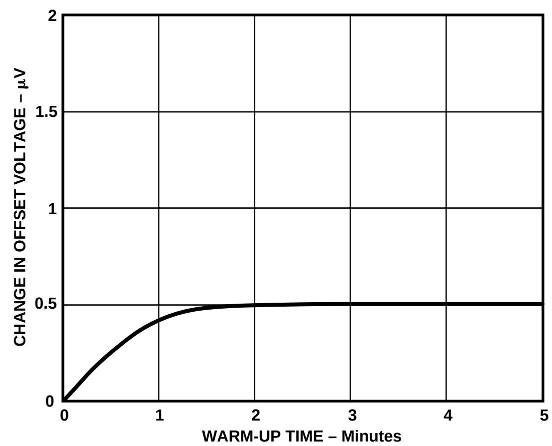


Figure 7. Change in Input Offset Voltage vs. Warm-Up Time

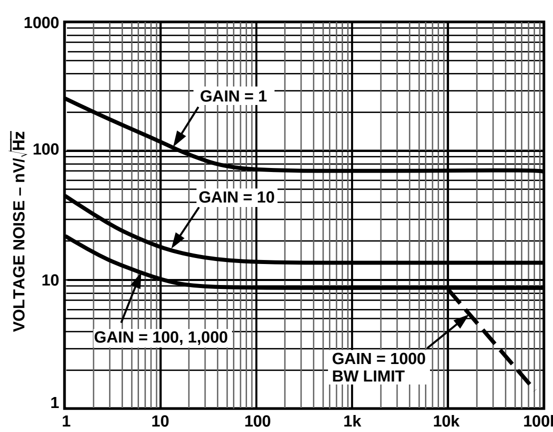


Figure 8. Voltage Noise Spectral Density vs. Frequency, (G = 1–1000)

AD620–Typical Characteristics

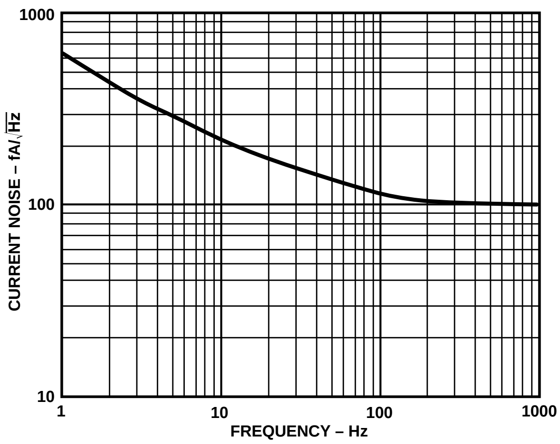


Figure 9. Current Noise Spectral Density vs. Frequency

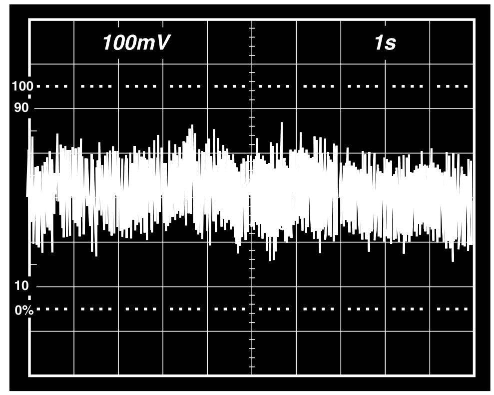


Figure 11. 0.1 Hz to 10 Hz Current Noise, 5 pA/Div

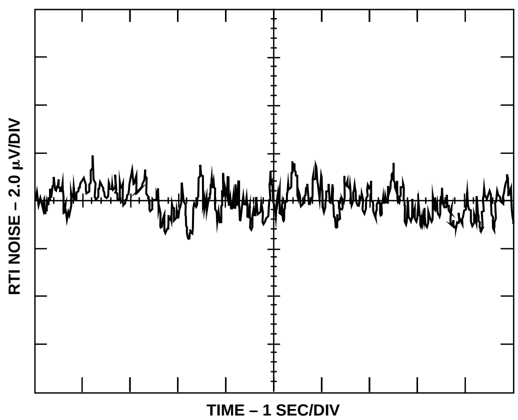


Figure 10a. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

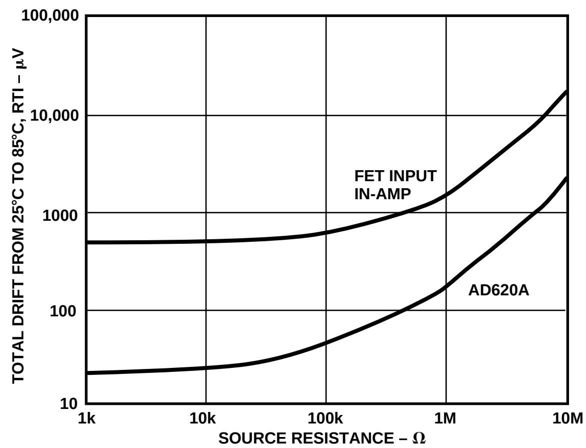


Figure 12. Total Drift vs. Source Resistance

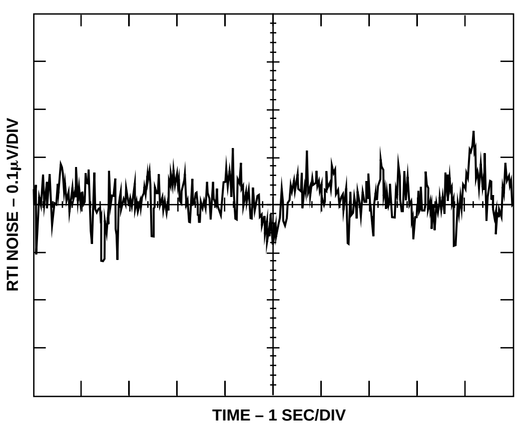


Figure 10b. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

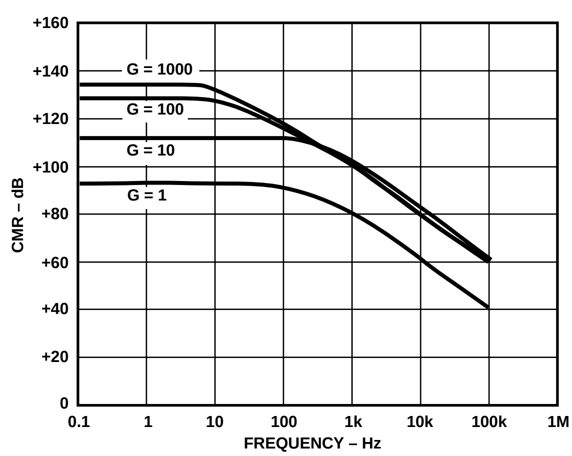


Figure 13. CMR vs. Frequency, RTI, Zero to 1 kΩ Source Imbalance

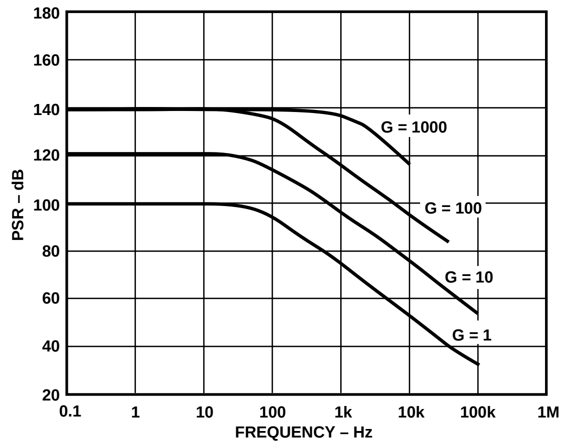


Figure 14. Positive PSR vs. Frequency, RTI (G = 1–1000)

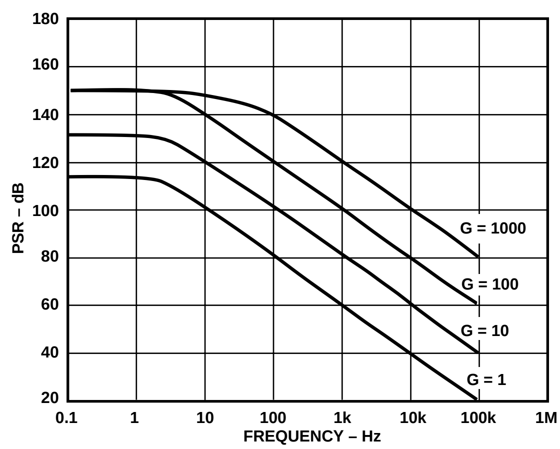


Figure 15. Negative PSR vs. Frequency, RTI (G = 1–1000)

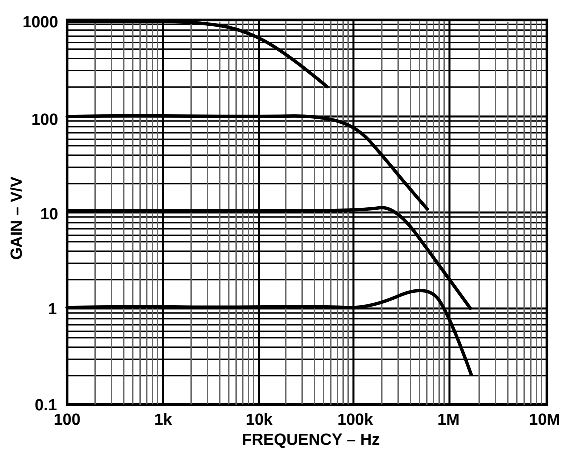


Figure 16. Gain vs. Frequency

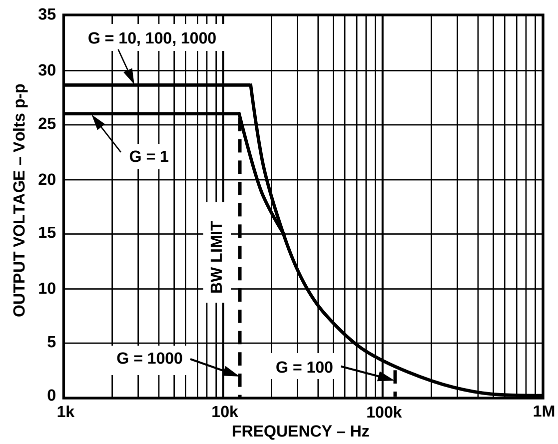


Figure 17. Large Signal Frequency Response

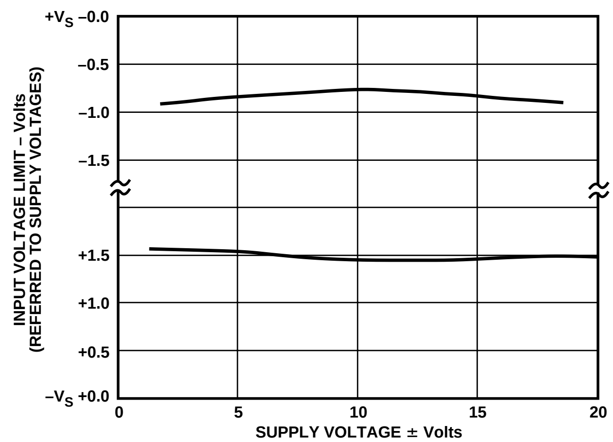


Figure 18. Input Voltage Range vs. Supply Voltage, G = 1

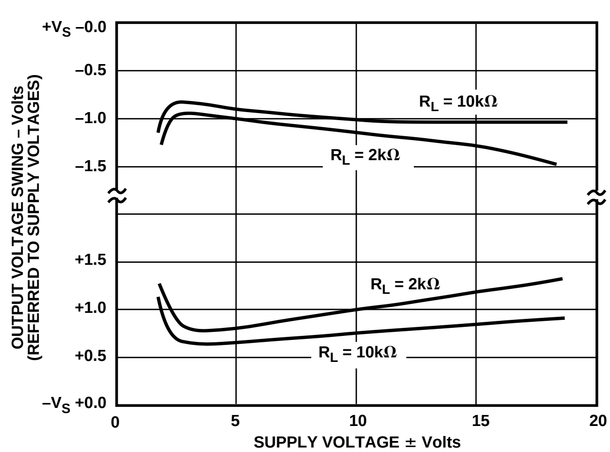


Figure 19. Output Voltage Swing vs. Supply Voltage, G = 10

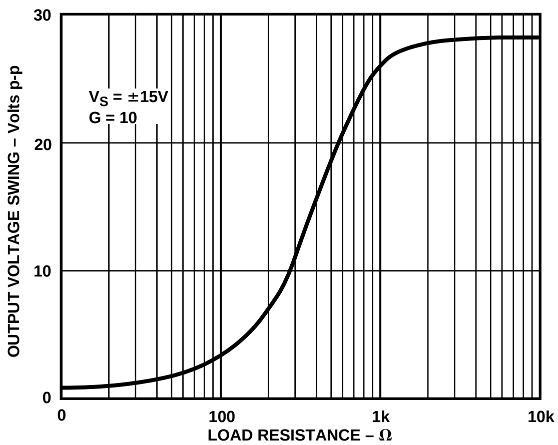


Figure 20. Output Voltage Swing vs. Load Resistance

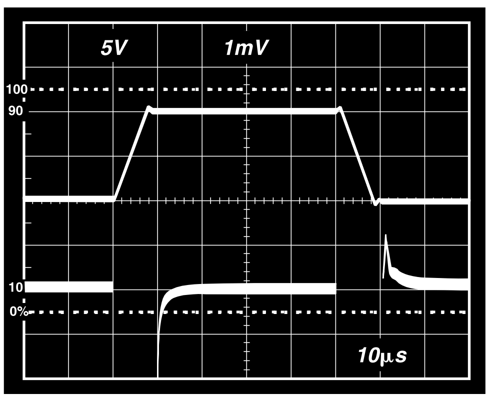


Figure 21. Large Signal Pulse Response and Settling Time G = 1 (0.5 mV = 0.01%)

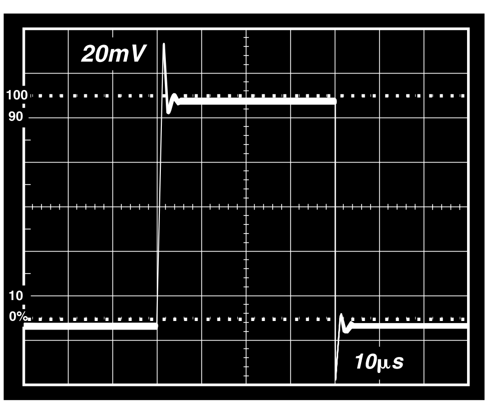


Figure 22. Small Signal Response, G = 1, R_L = 2 kΩ, C_L = 100 pF

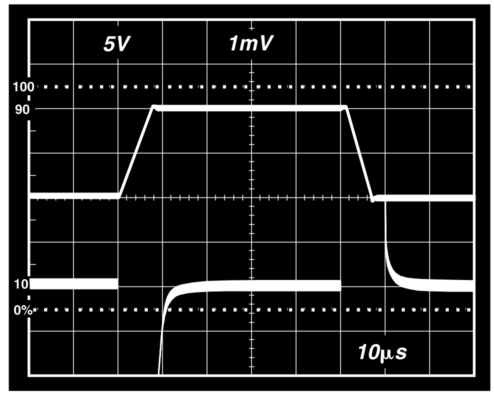


Figure 23. Large Signal Response and Settling Time, G = 10 (0.5 mV = 001%)

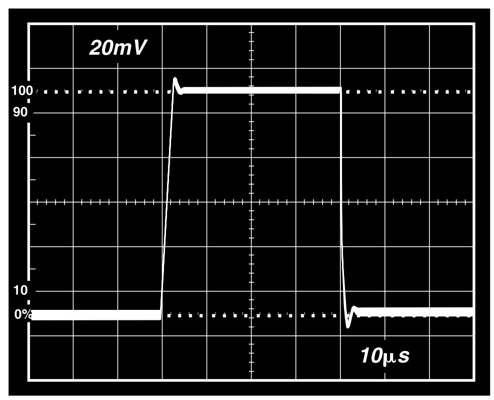


Figure 24. Small Signal Response, G = 10, R_L = 2 kΩ, C_L = 100 pF

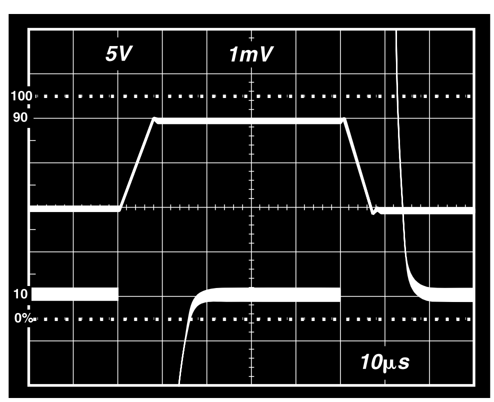


Figure 25. Large Signal Response and Settling Time, G = 100 (0.5 mV = 0.01%)

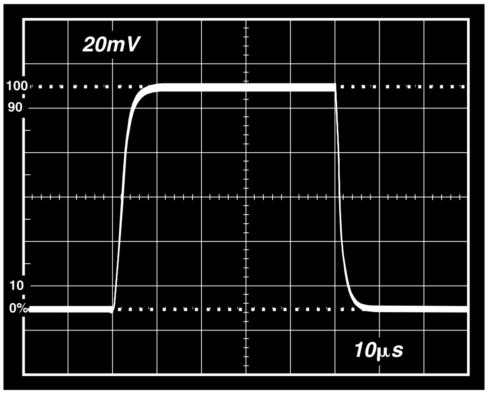


Figure 26. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

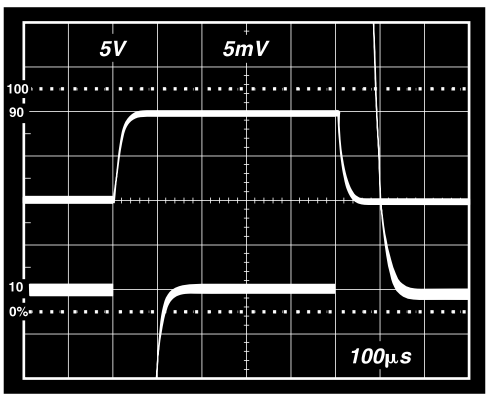


Figure 27. Large Signal Response and Settling Time, G = 1000 (0.5 mV = 0.01%)

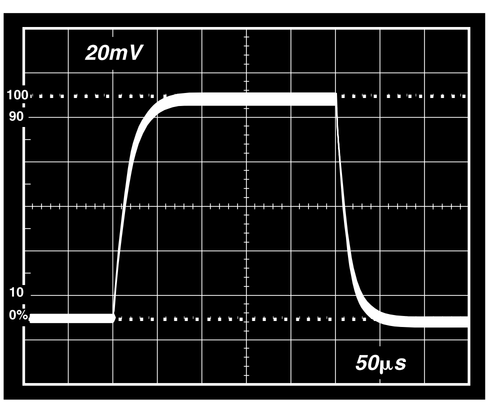


Figure 28. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, C_L = 100 pF

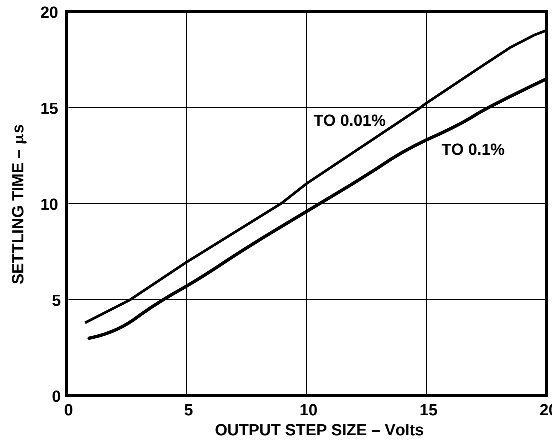


Figure 29. Settling Time vs. Step Size (G = 1)

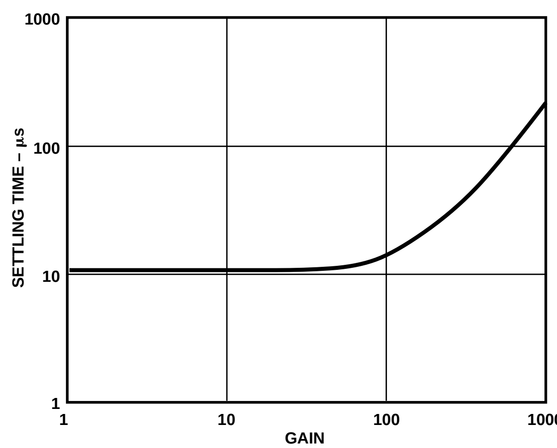


Figure 30. Settling Time to 0.01% vs. Gain, for a 10 V Step

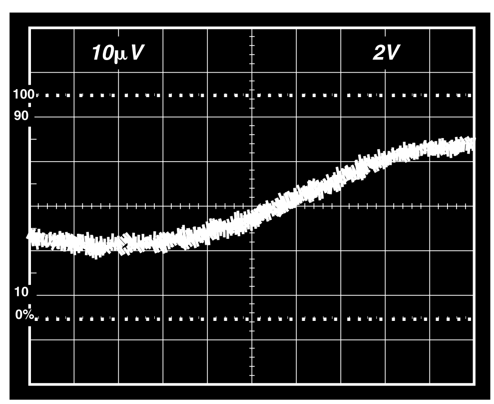


Figure 31a. Gain Nonlinearity, G = 1, R_L = 10 kΩ (10 μV = 1 ppm)

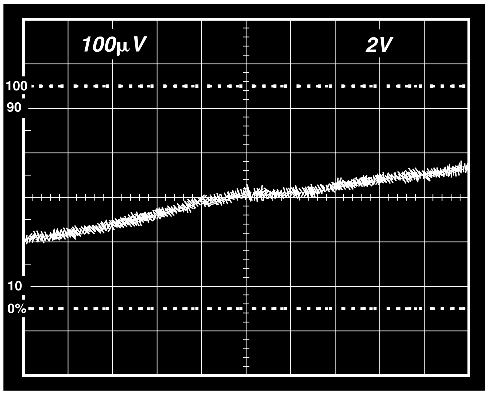


Figure 31b. Gain Nonlinearity, G = 100, R_L = 10 kΩ (100 µV = 10 ppm)

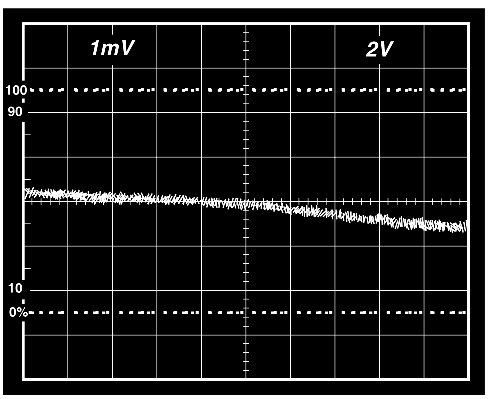


Figure 31c. Gain Nonlinearity, G = 1000, R_L = 10 kΩ (1 mV = 100 ppm)

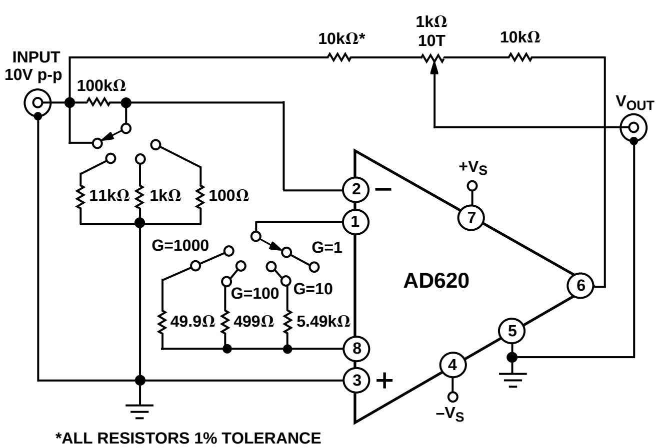


Figure 32. Settling Time Test Circuit

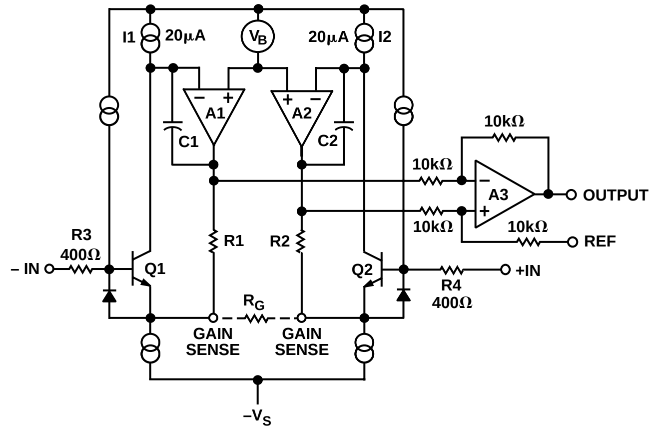


Figure 33. Simplified Schematic of AD620

THEORY OF OPERATION

The AD620 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain *accurately* (to 0.15% at G = 100) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus ensuring the high level of performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 33), yet offer 10× lower Input Bias Current thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1, Q2 thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by G = (R1 + R2)/R_G + 1. The unity-gain subtracter A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors. (b) The gain-bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/$\sqrt{Hz}$, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

so that

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

Make vs. Buy: A Typical Bridge Application Error Budget

The AD620 offers improved performance over "homebrew" three op amp IA designs, along with smaller size, fewer components and 10× lower supply current. In the typical application, shown in Figure 34, a gain of 100 is required to amplify a bridge output of 20 mV full scale over the industrial temperature range of –40°C to +85°C. The error budget table below shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system in which it is being used, the AD620 provides greater accuracy, and at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an autogain/autozero cycle will remove all absolute accuracy and drift errors leaving only the resolution errors of gain nonlinearity and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07 specifications for input voltage offset and noise have been multiplied by $\sqrt{2}$. This is because a three op amp type in-amp has two op amps at its inputs, both contributing to the overall input error.

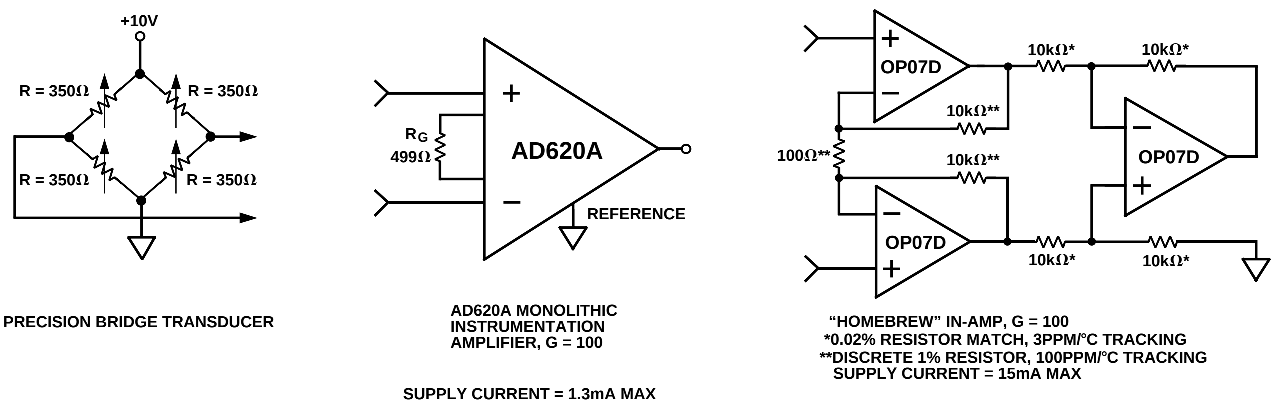


Figure 34. Make vs. Buy

Table I. Make vs. Buy Error Budget

Error Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale AD620	Homebrew
ABSOLUTE ACCURACY at T_A = +25°C				
Input Offset Voltage, µV	125 µV/20 mV	(150 µV × $\sqrt{2}$)/20 mV	6,250	10,607
Output Offset Voltage, µV	1000 µV/100/20 mV	((150 µV × 2)/100)/20 mV	500	150
Input Offset Current, nA	2 nA × 350 Ω/20 mV	(6 nA × 350 Ω)/20 mV	18	53
CMR, dB	110 dB→3.16 ppm, × 5 V/20 mV	(0.02% Match × 5 V)/20 mV/100	791	500
		Total Absolute Error	7,558	11,310
DRIFT TO +85°C				
Gain Drift, ppm/°C	(50 ppm + 10 ppm) × 60°C	100 ppm/°C Track × 60°C	3,600	6,000
Input Offset Voltage Drift, µV/°C	1 µV/°C × 60°C/20 mV	(2.5 µV/°C × $\sqrt{2}$ × 60°C)/20 mV	3,000	10,607
Output Offset Voltage Drift, µV/°C	15 µV/°C × 60°C/100/20 mV	(2.5 µV/°C × 2 × 60°C)/100/20 mV	450	150
		Total Drift Error	7,050	16,757
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz–10 Hz Voltage Noise, µV p-p	0.28 µV p-p/20 mV	(0.38 µV p-p × $\sqrt{2}$)/20 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,662	28,134

G = 100, V_S = ±15 V.

(All errors are min/max and referred to input.)

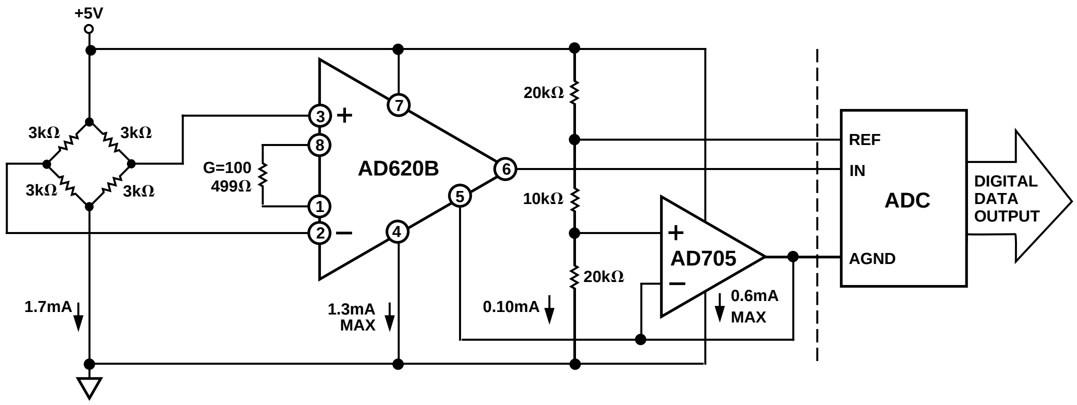


Figure 35. A Pressure Monitor Circuit which Operates on a +5 V Single Supply

Pressure Measurement

Although useful in many bridge applications such as weigh scales, the AD620 is especially suitable for higher resistance pressure sensors powered at lower voltages where small size and low power become more significant.

Figure 35 shows a 3 kΩ pressure transducer bridge powered from +5 V. In such a circuit, the bridge consumes only 1.7 mA. Adding the AD620 and a buffered voltage divider allows the signal to be conditioned for only 3.8 mA of total supply current.

Small size and low cost make the AD620 especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it will also serve applications such as diagnostic non-invasive blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 36) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-lead mini-DIP and SOIC package offerings make it an excellent choice for battery powered data recorders.

Furthermore, the low bias currents and low current noise coupled with the low voltage noise of the AD620 improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

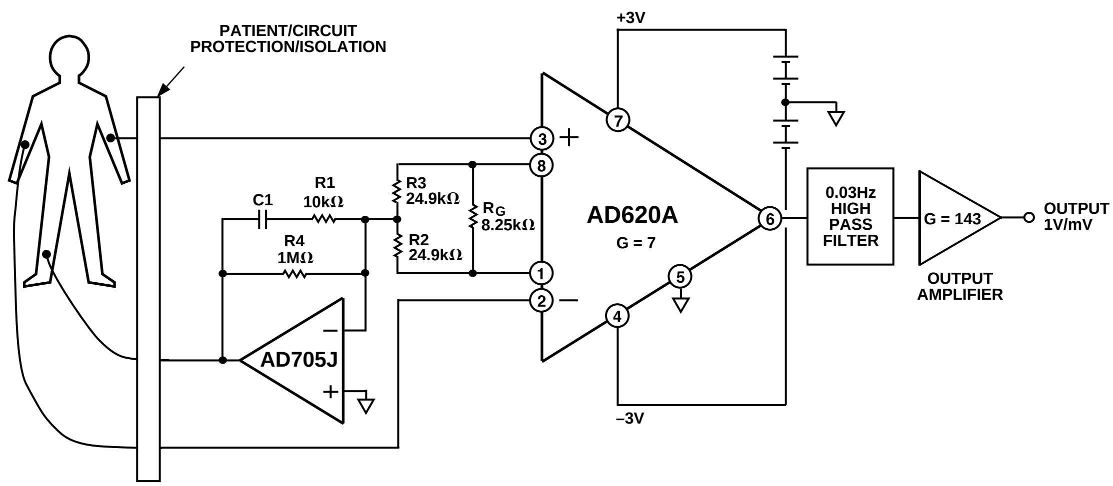


Figure 36. A Medical ECG Monitor Circuit

Precision V-I Converter

The AD620, along with another op amp and two resistors, makes a precision current source (Figure 37). The op amp buffers the reference terminal to maintain good CMR. The output voltage V_X of the AD620 appears across R1, which converts it to a current. This current less only, the input bias current of the op amp, then flows out to the load.

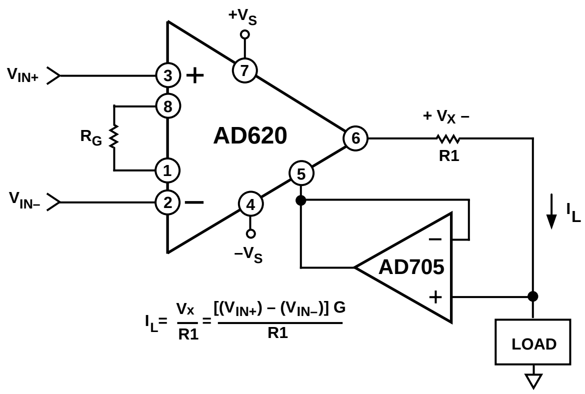


Figure 37. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

GAIN SELECTION

The AD620's gain is resistor programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620 is designed to offer accurate gains using 0.1%–1% resistors. Table II shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain R_G can be calculated by using the formula:

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

To minimize gain error, avoid high parasitic resistance in series with R_G; to minimize gain drift, R_G should have a low TC—less than 10 ppm/°C—for the best performance.

Table II. Required Values of Gain Resistors

1% Std Table Value of R_G, Ω	Calculated Gain	0.1% Std Table Value of R_G, Ω	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as:

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage, and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 features 400 Ω of series thin film resistance at its inputs, and will safely withstand input overloads of up to ±15 V or ±60 mA for several hours. This is true for all gains, and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For longer time periods, the current should not exceed 6 mA ($I_{IN} \leq V_{IN}/400\ \Omega$). For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an FD333) will reduce the required resistance, yielding lower noise.

RF INTERFERENCE

All instrumentation amplifiers can rectify out of band signals, and when amplifying small signals, these rectified voltages act as small dc offset errors. The AD620 allows direct access to the input transistor bases and emitters enabling the user to apply some first order filtering to unwanted RF signals (Figure 38), where RC ≈ 1/(2 πf) and where f ≥ the bandwidth of the AD620; C ≤ 150 pF. Matching the extraneous capacitance at Pins 1 and 8 and Pins 2 and 3 helps to maintain high CMR.

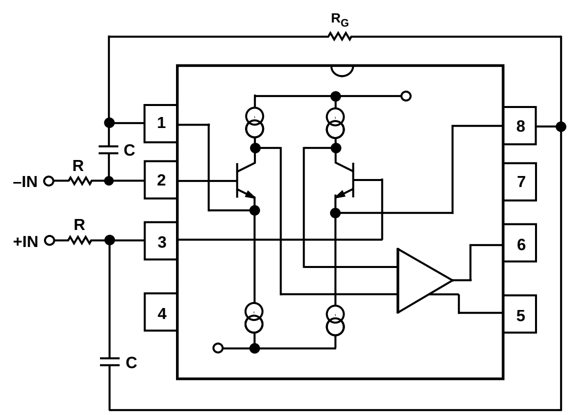


Figure 38. Circuit to Attenuate RF Interference

COMMON-MODE REJECTION

Instrumentation amplifiers like the AD620 offer high CMR, which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications shielded cables are used to minimize noise, and for best CMR over frequency the shield should be properly driven. Figures 39 and 40 show active data guards that are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

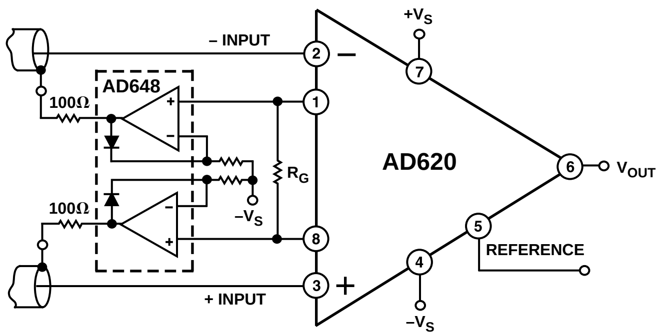


Figure 39. Differential Shield Driver

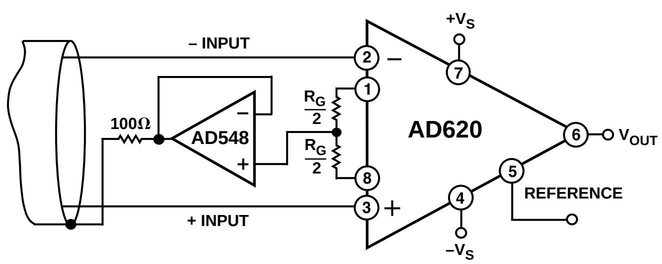


Figure 40. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 41). It would be convenient to use a single ground line; however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package as shown.

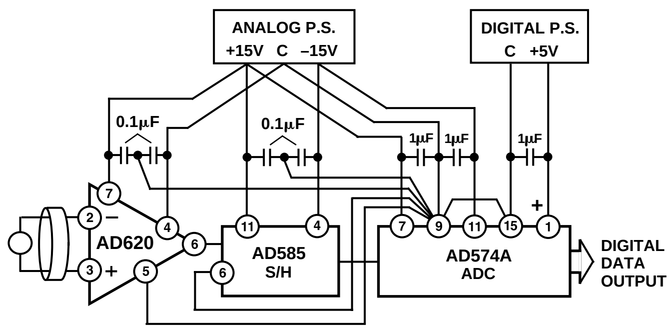


Figure 41. Basic Grounding Practice

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents; therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 42. Refer to the *Instrumentation Amplifier Application Guide* (free from Analog Devices) for more information regarding in amp applications.

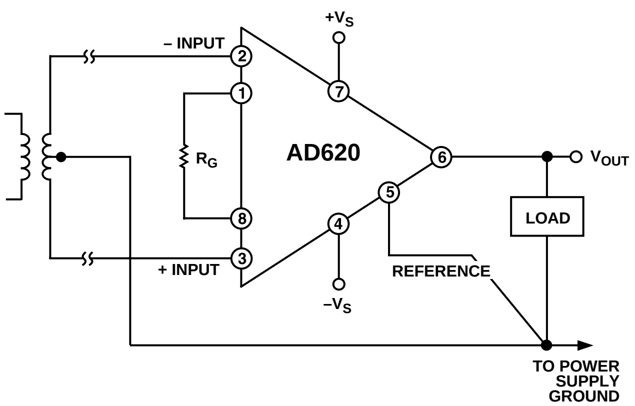


Figure 42a. Ground Returns for Bias Currents with Transformer Coupled Inputs

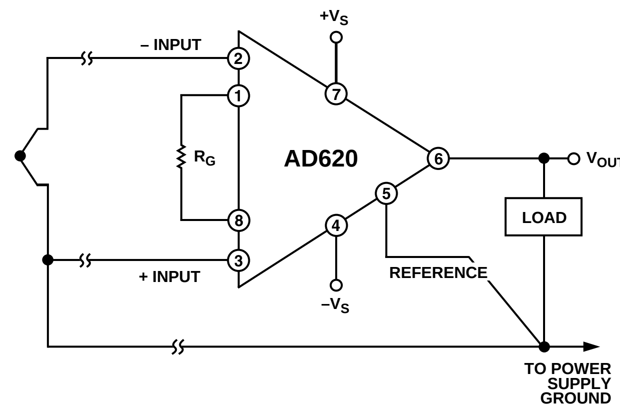


Figure 42b. Ground Returns for Bias Currents with Thermocouple Inputs

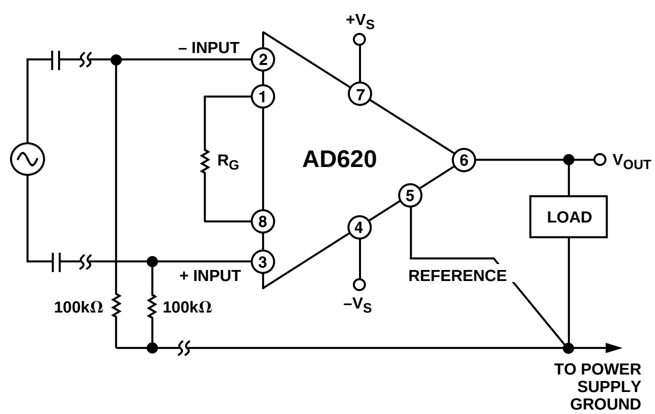
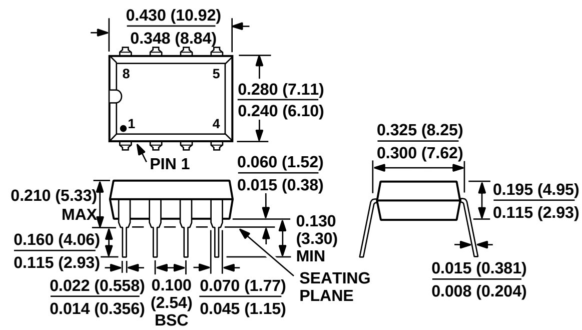


Figure 42c. Ground Returns for Bias Currents with AC Coupled Inputs

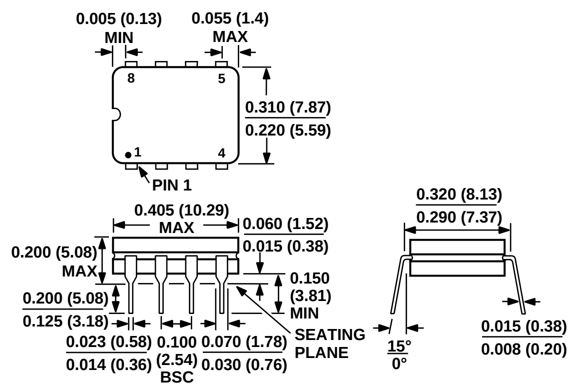
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

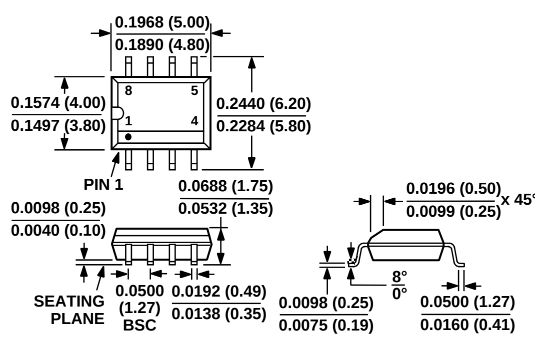
Plastic DIP (N-8) Package



Cerdip (Q-8) Package



SOIC (SO-8) Package



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